IN THE CLAIMS

1. (currently amended) An integrated circuit, comprising:

a semiconductor substrate including semiconductor devices;

a first wiring layer having an associated thickness being located over the substrate and having interconnect wire embedded therein;

a second wiring layer having an associated thickness being located on the first wiring layer and having interconnect wire embedded therein; and

a capacitor having a first metal-based charge-storage electrode, a second metal-based charge-storage electrode, and a dielectric layer interposed between the charge-storage electrodes, the charge-storage electrodes extending through the thickness of the second wiring layer and at least part of the first wiring layer wherein the capacitor is completely disposed in a window formed ~~in~~ through the thickness of the second wiring layer and at least part of the first wiring layer.

2. (original) The circuit of claim 1, wherein the dielectric layer comprises one of Ta_2O_5, $BaSrTiO_4$, Al_2O_3, ZrO_2, and HfO_2.

3. (original) The circuit of claim 1, wherein

a first region of the substrate includes dynamic random access memory cells;

a second region of the substrate includes logic circuits and is physically separate from the first region; and

the capacitor is located in a portion of the wiring layers located over the first region of the substrate.

4. (original) The circuit of claim 3, wherein the capacitor is a functional portion of one of the random access memory cells.

5. (original) The circuit of claim 1, further comprising:

a third wiring layer being located on the second wiring layer and having metal-based interconnect wire embedded therein, the first charge-storage electrode of the capacitor being in

physical contact with a portion of the interconnect wire of the third layer.

6. (original) The circuit of claim 1, further comprising:

a tungsten plug being located between the second charge-storage electrode and a portion of the substrate.

7. (original) The circuit of claim 1, wherein at least one of the wiring layers is a dual damascene wiring layer.

8. (original) The circuit of claim 1, further comprising:

a transistor located on the substrate; and

a metal plug electrically connecting the second charge-storage electrode to one of a source and a drain of the transistor.

(9-24 canceled)